First Named Inventor	Frankie F. Roohparvar	**PRE-APPEAL BRIEF REQUEST FOR REVIEW**
Serial No.	09/838,764	
Filing Date	April 19, 2001	
Group Art Unit	2133	
Examiner Name	Mujtaba K. Chaudry	
Confirmation No.	1344	
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Title: MEMORY WITH ELEMENT REDUNDANCY		

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In response to the Final Office Action mailed March 16, 2006 and the Advisory Action mailed on June 1, 2006, please consider the following in the Pre-Appeal Brief Request for Review:

REMARKS

Status of the Clams

The amendments to claims 8, 11-12, 16-17, 19-20, 22, 24, 28, and 30 were not entered for purposes of appeal. The purpose of these amendments by the Appellant were to attempt to overcome the rejection of claims 1-30 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-37 of U.S. Patent No. 6,469,932. As such the double patenting rejection as to claims 8-30 will not be addressed herein. However, Appellant will address the double patenting rejection as to claims 1-7, as detailed below.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nozoe et al. (U.S. Patent No. 6,351,412) and further in view of Mizuno et al. (U.S. Patent No. 5,357,473). Appellant respectfully traverses the basis for this rejection and feels that claims 1-30 are allowable for the following reasons.

Appellant's disclosed invention claims a non-volatile memory device with a memory array having primary and redundant memory cells, where a redundant fuse circuitry or register of the memory device is used to replace the primary memory cells with the redundant memory cells and the redundant fuse or register circuitry stores an error code indicating a type of defect in the primary memory cells in addition to the address of the defective primary memory cells in the array. Appellant respectfully submits herein that Nozoe et al. and Mizuno et al. do not teach or suggest all elements of the Appellant's claimed invention either alone or in combination.

In maintaining the rejection of claims 1-30, the Examiner disagreed with Appellant's assertion contained in the Response mailed May 16, 2006 that Nozoe et al. and Mizuno et al. do not teach or suggest storing an error code indicating a type of error in a memory array, either alone or in combination. In support of this, the Examiner stated in the Final Office Action mailed March 16, 2006 that " ... Nozoe *does not explicitly teach* storing an error code that indicated the type of error. ... Although Nozoe is deficient in teaching this specific limitation, an analogous art, Mizuno was introduced. Mizuno teaches a semiconductor storage system that comprises ... a defect address memory for storing and outputting information on an address where at least one defective bit exists and an alternate address to be substituted for said address, and a defect address manipulating circuit for substituting said alternate address for said address

where said defective bit exists in accordance with an output of said defect address memory. ... In particular, Mizuno teaches (col. 8, lines 54-68) *identifying various type of defects and classifying them accordingly.* Applicant also contends that Mizuno does not teach or suggest. '...storing the type of error...' The Examiner respectfully disagrees. Mizuno teaches (col. 8, lines 54-55, further in col. 10, lines 1-58) *the defects are classified into four types.*" Final Office Action, page 3, first paragraph (emphasis added).

Appellant respectfully contends that the statement by the Examiner regard to Nozoe et al. is an admission that Nozoe et al. does not teach or suggest storing an error code indicating the type of error. *See, e.g.*, Nozoe et al., column 1, line 62 to column 2, line 2, column 2, lines 33-67, and column 10, lines 32-37. Appellant respectfully contends that the statement by the Examiner regard to Mizuno et al. while describing the possible types of array errors and how to detect them for replacement with a spare redundant element, does not teach or suggest storing an error code indicating the type of error in the replaced element. In fact, Mizuno et al. discloses only storing the addresses of defective elements to be replaced with spare redundant elements Mizuno et al. makes not mention of storing a code indicating a type of defect, and, further, would have to be modified to store such an error code to be associated with the stored defective address. Appellant's independent claims 1, 8, 12, 17, 20, 24 and 28 each require storing an error code that indicates a specific type of error, Appellant thus respectfully submits that the Office has failed to make a *prima facie* showing of obviousness of any of Appellant's claims as neither reference teaches or suggests at least this limitation. *See, e.g.,* Mizuno et al., Figure 3, column 3, lines 19-59; column 4, lines 26-53; column 8, line 33 to column 9, line 39 and column 9, line 64 to column 10, line 47.

Appellant thus respectfully maintains that combining Nozoe et al. with Mizuno et al. does not teach or suggest the Appellant's claimed invention, as maintained by the Examiner. Appellant therefore respectfully contends that Mizuno et al. and Nozoe et al. do not teach or suggest all elements of the Appellant's claimed, either alone or in combination.

Because it appears that Appellant's arguments have overcome the rejections contained in the Final Office Action mailed March 16, 2006, and because Appellant respectfully contends that the Examiner has not met the burden of establishing a *prima facie* case of obviousness in regards to claims 1, 8, 12, 17, 20, 24 and 28, and, in addition, that claims 1, 8, 12, 17, 20, 24 and 28 as pending have been shown to be patentably distinct from the cited references Nozoe et al. and

Mizuno et al. either alone or in combination, or alone or in combination with the Examiner's taking of official notice or inherency. As claims 2-7, 9-11, 13-16, 18-19, 21-23, 25-27 and 29-30 depend from and further define claims 1, 8, 12, 17, 20, 24 and 28, respectively, they are also believed to be allowable. Accordingly, Appellant contends that it is entitled to either withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-30 or a new action on the merits of the claims.

Double Patenting Rejection

Claims 1-30 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-37 of U.S. Patent No. 6,469,932. Amended claims 8, 11-12, 16-17, 19-20, 22, 24, 28, and 30 were not entered for purposes of appeal. However, Appellant respectfully traverses the basis for this rejection in regards to claims 1-7 and feels that they are allowable for the following reasons.

The Examiner stated in the Office Action mailed on September 16, 2005 that "[a]lthough the conflicting claims are not identical, they are not patentably distinct from each other. ... Patent '932 teaches a flash memory device comprising: a memory array; a state machine to control operations to the memory array; and a defect register to store data indicating a type of defect, wherein the state machine increments row addresses during an erase operation based on the type of defect stored in the defect register. ... Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to correct defective memory cells by redundant cells within the method and apparatus of patent '932." In the Final Office Action mailed on March 16, 2006 the Examiner maintained the rejection.

Appellant disagrees and respectfully maintains that claims 1-37 of the '932 Patent do not teach or suggest claims 1-7 of the Present Application. Specifically, Appellant respectfully maintains that claims 1-37 of the '932 Patent do not teach or suggest a flash memory having redundant fuse circuitry used to replace the primary memory cells with the redundant memory cells, wherein the redundant fuse circuitry stores an error code indicating a type of defect in addition to a defect location and contends that the flash memory device of claims 1-7 of the Present Application differ from that disclosed in claims 1-37 of the '932 Patent. In particular, Appellant respectfully maintains that claims 1-37 of the '932 Patent do not teach or suggest fuse or antifuse circuitry to hold the defect code and defective element address, only a register. In addition, Appellant respectfully maintains that claims 1-37 of the '932 Patent do not teach or

suggest replacing multiple types of defective elements from the memory array, only replacing a defective row with a redundant row. Appellant further maintains that the Examiner is impermissibly relying on the disclosure to provide the other missing defective elements, such as redundant fuse circuits and defective columns. *See,* MPEP § 804. The Appellant therefore maintains that claims 1-37 of the '932 Patent do not teach or suggest all elements of claims 1-7.

Because it appears that Appellant's arguments have overcome the rejections to claims 1-7 contained in the Final Office Action mailed March 16, 2006, and because there are no amendments to claims 1-7, Appellant contends the Office has provided no reasoned basis to maintaining rejection of claims 1-7 under the judicially created doctrine of obviousness-type double patenting. Therefore, Appellant maintains that claims 1-7 of the present application are patentably distinct from claims 1-37 of the '932 Patent because claims 1-7 of the present application require non-obvious limitations not included in claims 1-37 of the '932 Patent. Accordingly, Appellant contends that it is entitled to either withdrawal of the rejection under the judicially created doctrine of obviousness-type double patenting and allowance of claims 1-7 or a new action on the merits of the claims.

CONCLUSION

In view of the above remarks, Appellant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner or the review panel has any questions or concerns regarding this application or request, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 6/16/06

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